

REMARKS

Claims 1-25 are pending. Claims 1, 11 and 21 have been amended

Specification

The specification has been amended to delete the word "the" as suggested by the Examiner. The specification has also been amended to overcome the Examiner's objection to Figure 4. In particular, the reference "170" has been added to the paragraph.

Drawings

Figure 2 has been amended to remove reference signs 138, 142, 144, 146 and 158.

Claim Rejections – 35 U.S.C. §103

The Examiner asserted that claims 1, 2, 4, 6-8, 10-12, 14, 16-18, 20-22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (U.S. Patent 6,144,387) in view of Smith et al. (U.S. Patent 6,424,345 B1). Applicant respectfully disagrees with the Examiner's assertions. In particular, claims 1-25 fail to teach or suggest "defining a visible region in screen coordinates using a first rectangle, wherein the first rectangle handles color buffer resolutions larger than could be otherwise accommodated by image limits; handling buffer resolutions using a second rectangle and an area threshold, wherein the second rectangle is used for trivial rejection."

The present invention provides:

"Graphics-binning engine 126 (FIG. 2) uses two rectangles in the process of determining primitive-zone intersections: bin array rectangle 184 and binner clipping rectangle 186. Both of these rectangles 184, 186 are defined by graphics device state variables containing the screen-space location of the rectangle corners. Binner clipping rectangle 186 is used to define the visible region in screen coordinates. In most cases, the binner clipping rectangle 186 will coincide with the extent of color buffer 178 (FIG. 4), though one skilled in the art will recognize that this is not a requirement. Objects completely outside binner clipping rectangle 186 in one or more directions will be discarded. Objects that cannot be discarded will be subject to bin determination.

Bin array rectangle 184 is supported to handle color buffer resolutions larger than could otherwise be accommodated by the optimally-renderer image limits. If this threshold is exceeded, some portions of the scene will be rendering non-optimally. The non-optimal rendering is caused by rendering zones 182 larger than the optimal (cache-sized) zone size, where additional color/Z bandwidth may be required as the render cache 110 cannot contain the color and depth values for the enlarged zones.

When the color buffer resolution is at or below the threshold(s) (i.e., optimal conditions), bin array rectangle 184 is programmed to include all the zones 182 spanned by the binner clipping rectangle 186 (which should itself coincide with color buffer 178). Bin array rectangle 184 is positioned using the following rules:

- The origin (Xmin, Ymin) corner of bin array rectangle 184 is aligned to a zone 182; and
- The (inclusive) width of bin array rectangle 184 is a multiple of the zone width.

However, the binner clipping rectangle 186 is used for trivial rejection and its maximum values need not be zone-aligned. In the case where binner clipping rectangle 186 maximum values are positioned within a zone 182, bin array rectangle 184 must still extend out to the zone boundaries. As shown in FIG. 5, bin array rectangle 184 maximum values would extend past binner clipping rectangle 186 maximum values to include the full zone extent along those edges."

Neither Liu or Smith, alone or in combination, teaches or suggests a first rectangle that handles color buffer resolutions larger than could be otherwise accommodated by image limits. Liu merely discloses a visible region. Moreover, the cited references fail to teach or suggest a second rectangle for handling buffer resolutions. Applicant respectfully disagrees with the Examiner's assertion that the "second rectangle" is similar to the guard memory boundaries that store pixel color data. The cited references fail to disclose bin array and bin clipping rectangles that operate in conjunction to determine primitive-chunk intersections as claimed.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance.

The required fee for a three month extension of time is enclosed. Should it be Y determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666.

If the Examiner has any questions, she is invited to contact the undersigned at (310) 252-7605. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

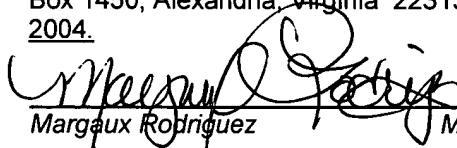
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By 
Farzad E. Amini, Reg. No. 42,261

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12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Fee Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on March 26, 2004.


Margaux Rodriguez March 26, 2004